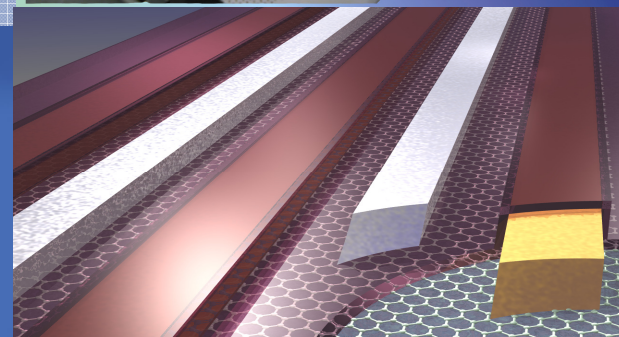
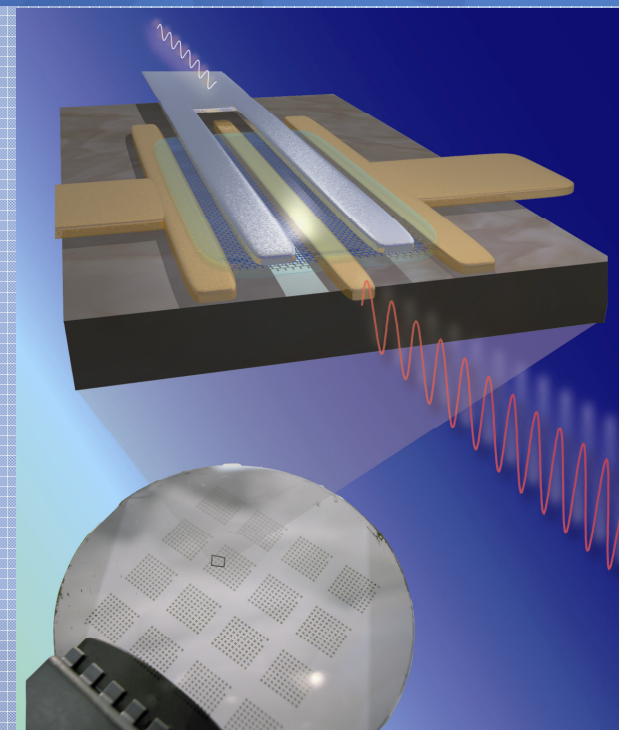




IBM Research | Science & Technology

IBM Nanoelectronics / Nano-system Strategy and Wafer Scale Graphene Nanoelectronics

C.Y Sung
Nanoelectronics Program Manager
IBM T.J. Watson Research Center
Science and Technology Strategy Department



Integrated Nanosystems Challenges-Opportunities

Workshop Objectives:

Realize heterogeneous smart nanosystems: provide active and intelligent complex functionalities (sense, communicate, remember and actuate) based on nanoscale phenomena, (eg. biologically inspired and hierarchical designs)

IBM Experiences:

Micro/Macroscale systems engineering:

- Design nanosystem structure for manufacturability**
- Plan and supply of elements**
- Model and integrate process**
- Nanoscale process control and optimization**

Common Goals:

Process engineering to scale-up and build for nano-manufacturing, nano-factory and nano-assembly to integrate nanoscale devices and systems

Outline

- **IBM Nanoelectronics Strategy**
 - Pushing to Si CMOS Limits
 - Subnanosystem Solutions
 - Post CMOS Carbon Electronics Opportunities
- **Applications**
- **Conclusions**

Outline

- **IBM Nanoelectronics Strategy**
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- Conclusions

Technical Transition Plan



Fundamental Research

Screen new materials & processes

IBM Almaden & Yorktown



Advanced Semiconductor R&D

Innovation in integrated device & process technology

Albany Nanotech Center



Technology Development

Multi-company co-located joint development

IBM East Fishkill

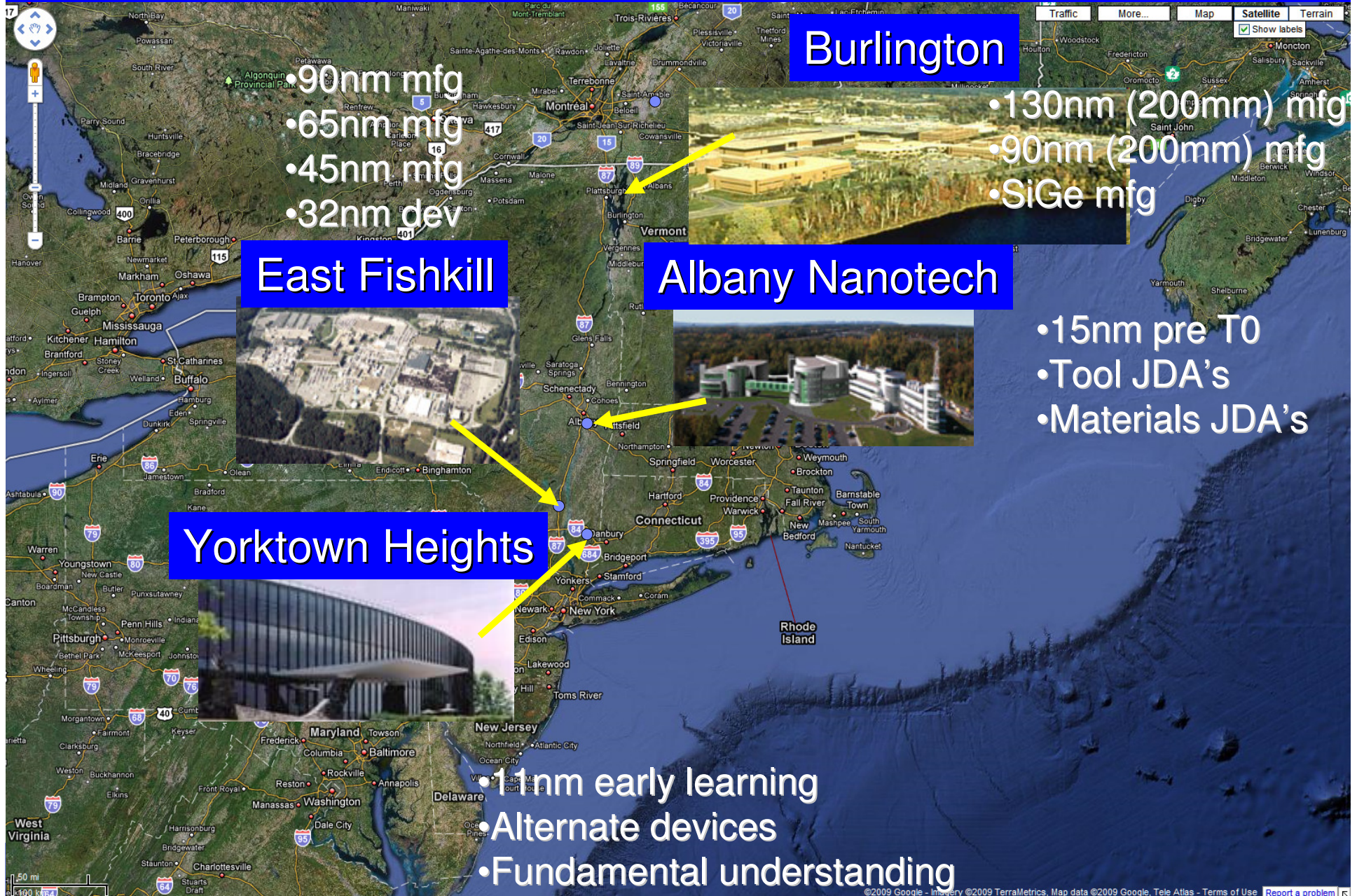


Manufacturing

Process synchronized fabricators (GDSII compatible)

USA

IBM Semiconductor Research, Development and Manufacturing Sites

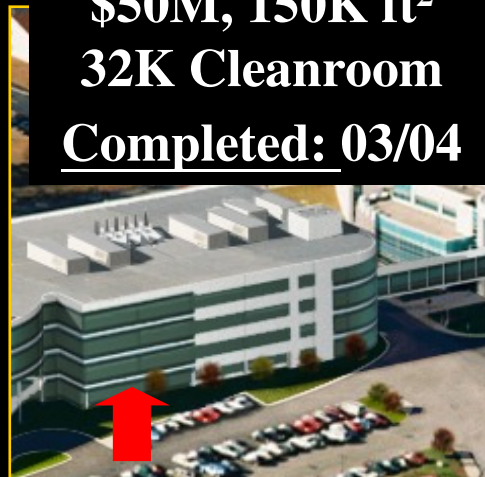


IBM –SUNY Albany Nanotech Center

State-of-the-Art Infrastructure

NanoFab 300S

\$50M, 150K ft²
32K Cleanroom
Completed: 03/04



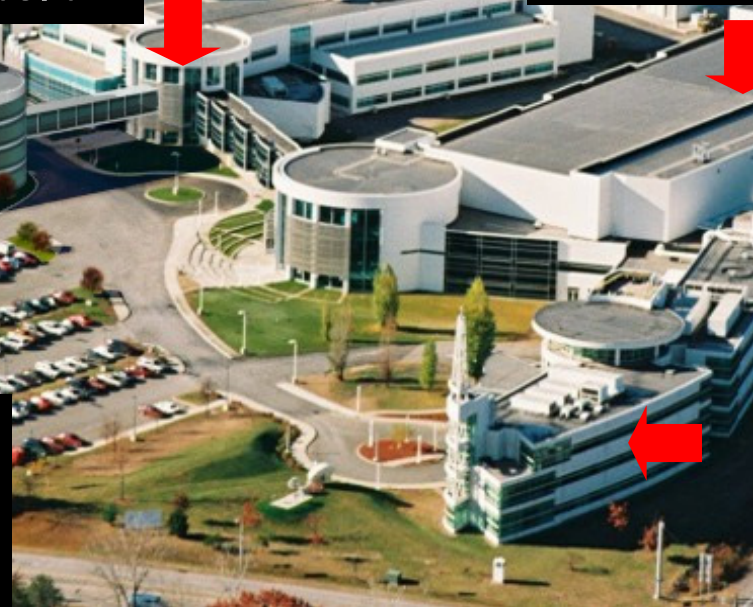
NanoFab 300N

\$175M, 228K ft²
35K Cleanroom
Completed: 12/05



NanoFab 300E

\$100M, 250K ft²
15K Cleanroom
Completed: 05/09



NanoFab 200

\$16.5M, 70K ft²
4K Cleanroom
Completed: 06/97

IBM Albany Nanotech has 80,000 ft² 300mm Wafer Cleanrooms with \$4.5B Cutting-edge Facilities

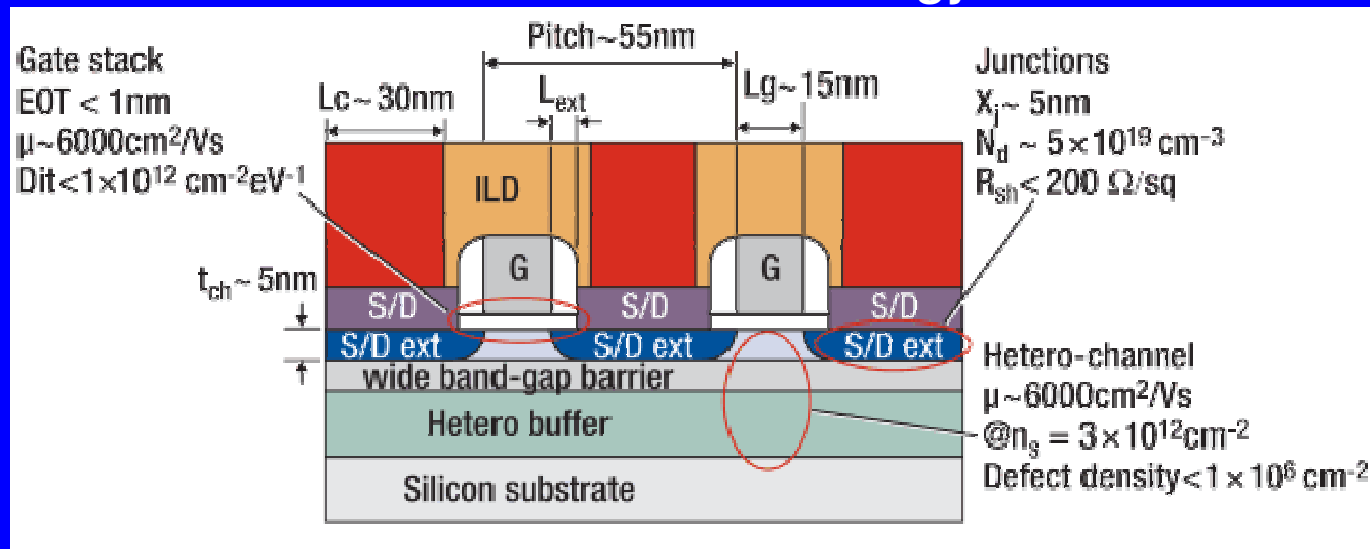
Outline

- IBM Nanoelectronics Strategy
 - Pushing Si CMOS to Limits
 - Subsystem Solutions
 - Post CMOS Carbon Electronics Opportunities
- Applications
- Conclusions

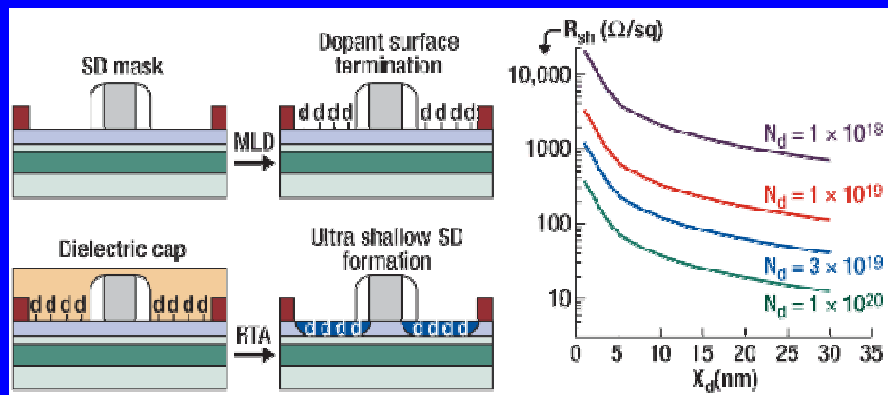
High Mobility III-V Channel Materials

(from Sematech)

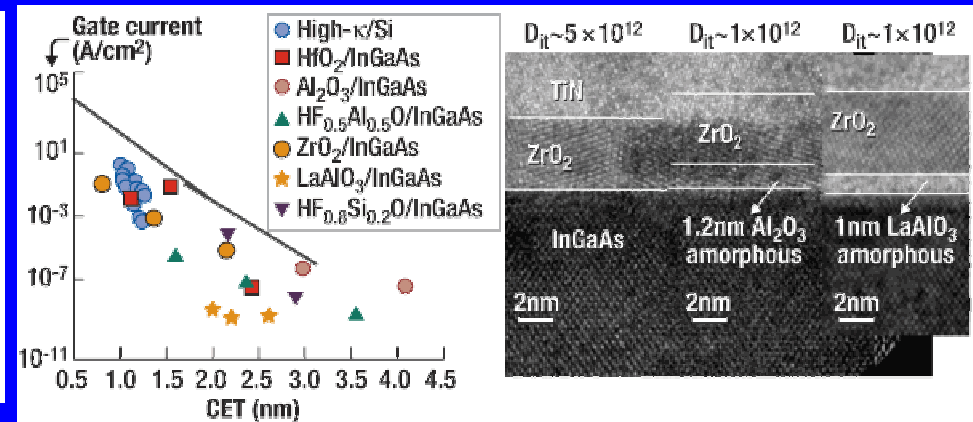
nFET 15nm technology



Mono-layer doping

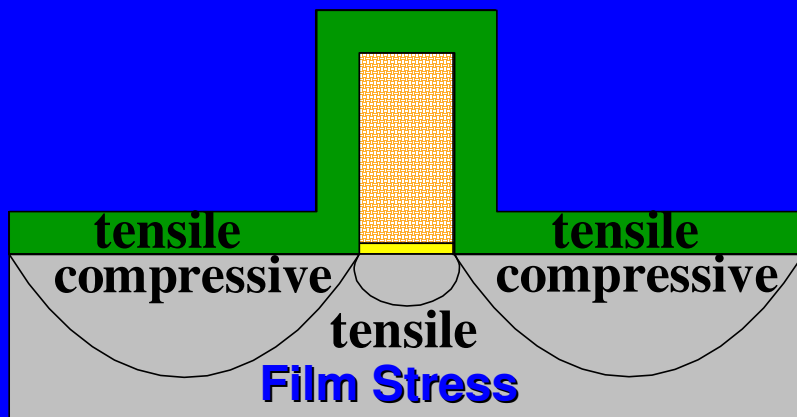
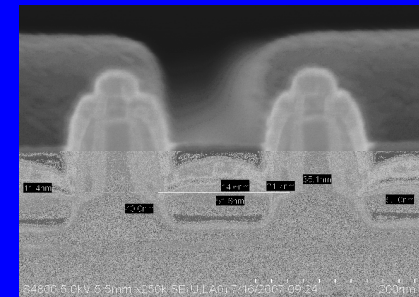
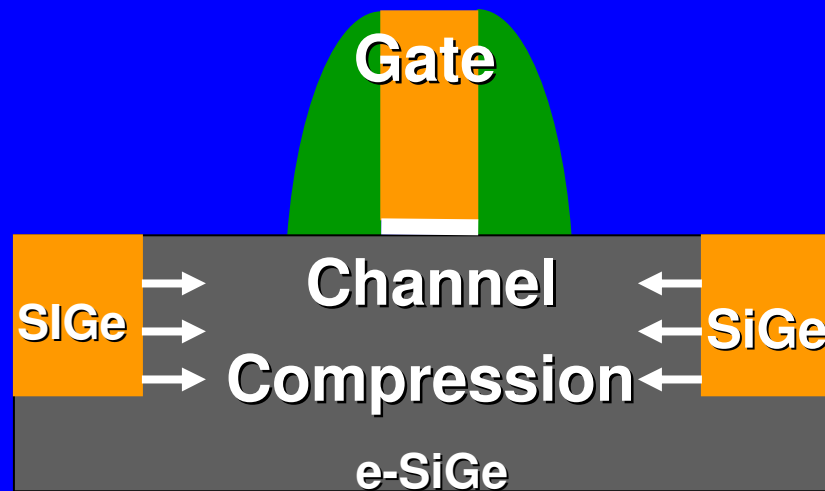


High-k gate on In0.53Ga0.47As



Mobility Enhancement Techniques

Strain & Substrate Engineering to give mechanical Stress enabled performance improvements



Device Count

Node	Device Pitch (nm)	Transistors / cm ²	Transistors in 450 mm ²	Year
45	170-180	0.4 B	1.8 B	2008
32	130	0.8 B	3.6 B	2010
22	100	~1.6 B	7.2 B	2012
15	80 - 56	~3.2 B	14.4 B	2014
11	50 - 40	~6.4 B	25.8 B	2016
8	35 - 28			
5	25 - 20			

• Add 3D integration

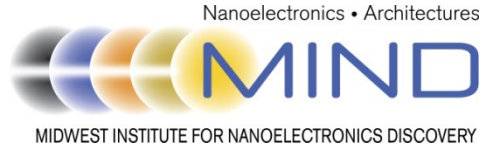
100 Billion Transistor/Chip
Do we need it? How to use them?

Outline

- IBM Nanoelectronics Strategy
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 - **Post CMOS Carbon Electronics Opportunities**
- Applications
- Conclusions



4 NRI Centers and Funded Universities



★ **Notre Dame**
Illinois-UC
Michigan
Cornell

Purdue
Penn State
UT-Dallas
GIT



★ **SUNY-Albany**
Purdue
Caltech
Yale

GIT
RPI
MIT
UVA

Harvard
Columbia
NCSU

WIN Western Institute of Nanoelectronics
★ **UC Los Angeles**
UC Berkeley
UC Irvine
UC Santa Barbara
Stanford
U Denver
Portland State
U Iowa

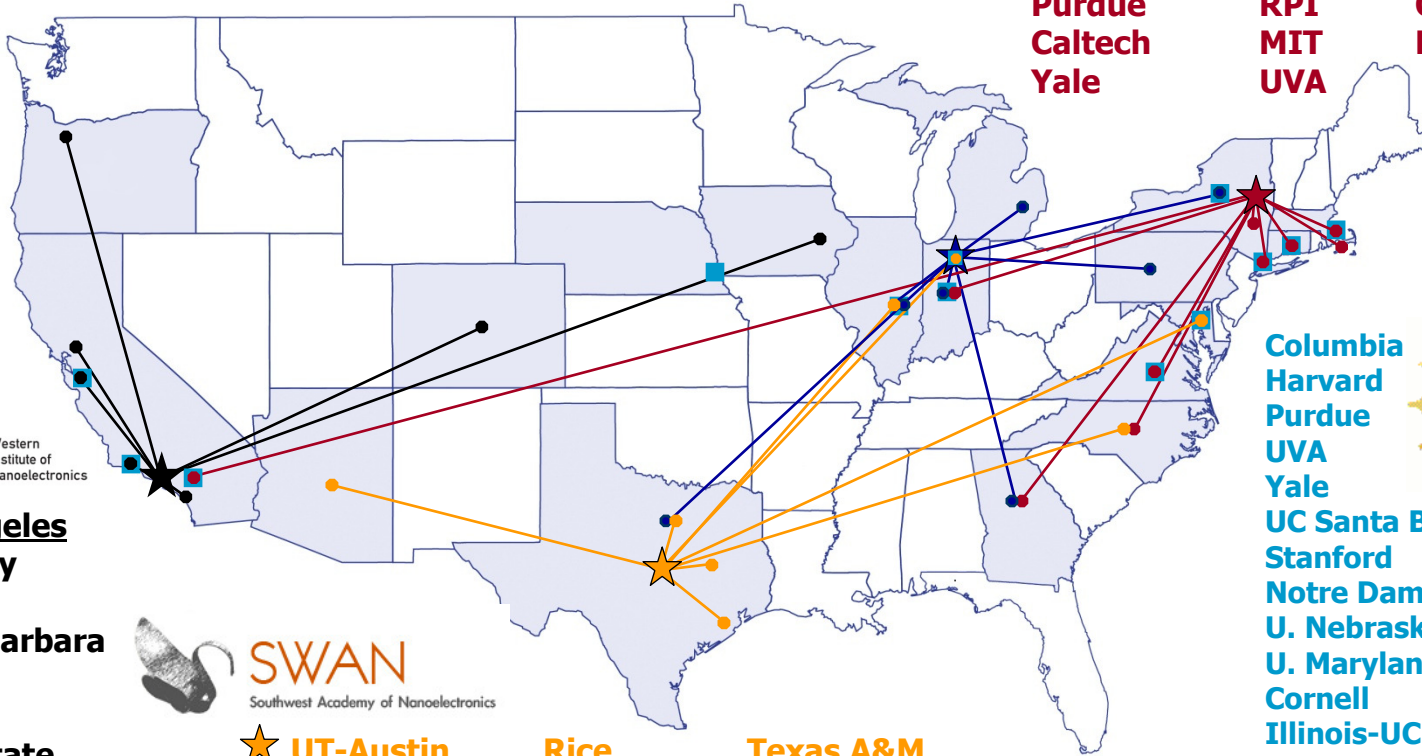


★ **UT-Austin**
UT-Dallas
U. Maryland

Rice
ASU
NCSU

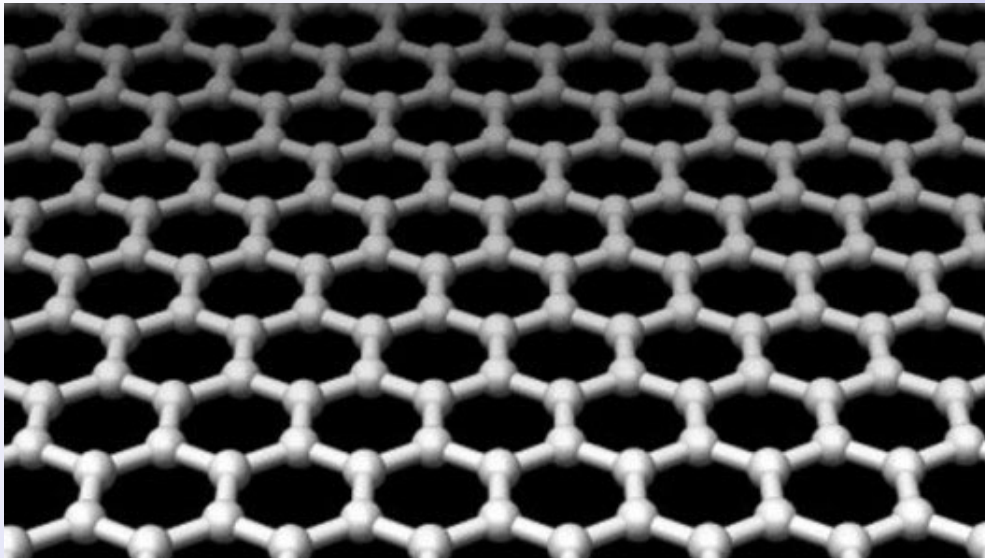
Texas A&M
Notre Dame
Illinois UC

Columbia
Harvard
Purdue
UVA
Yale
UC Santa Barbara
Stanford
Notre Dame
U. Nebraska/Lincoln
U. Maryland
Cornell
Illinois-UC
Caltech



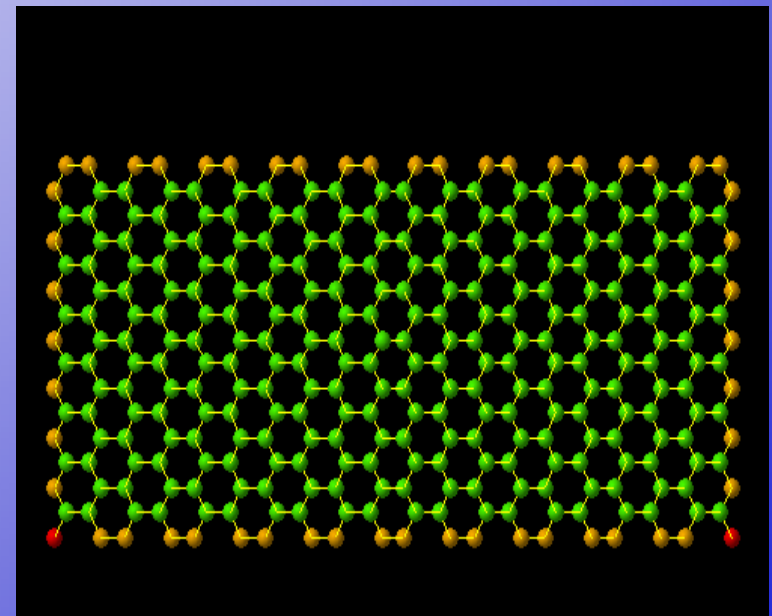
Over 30 Universities in 18 States

Graphene and Carbon Nanotube

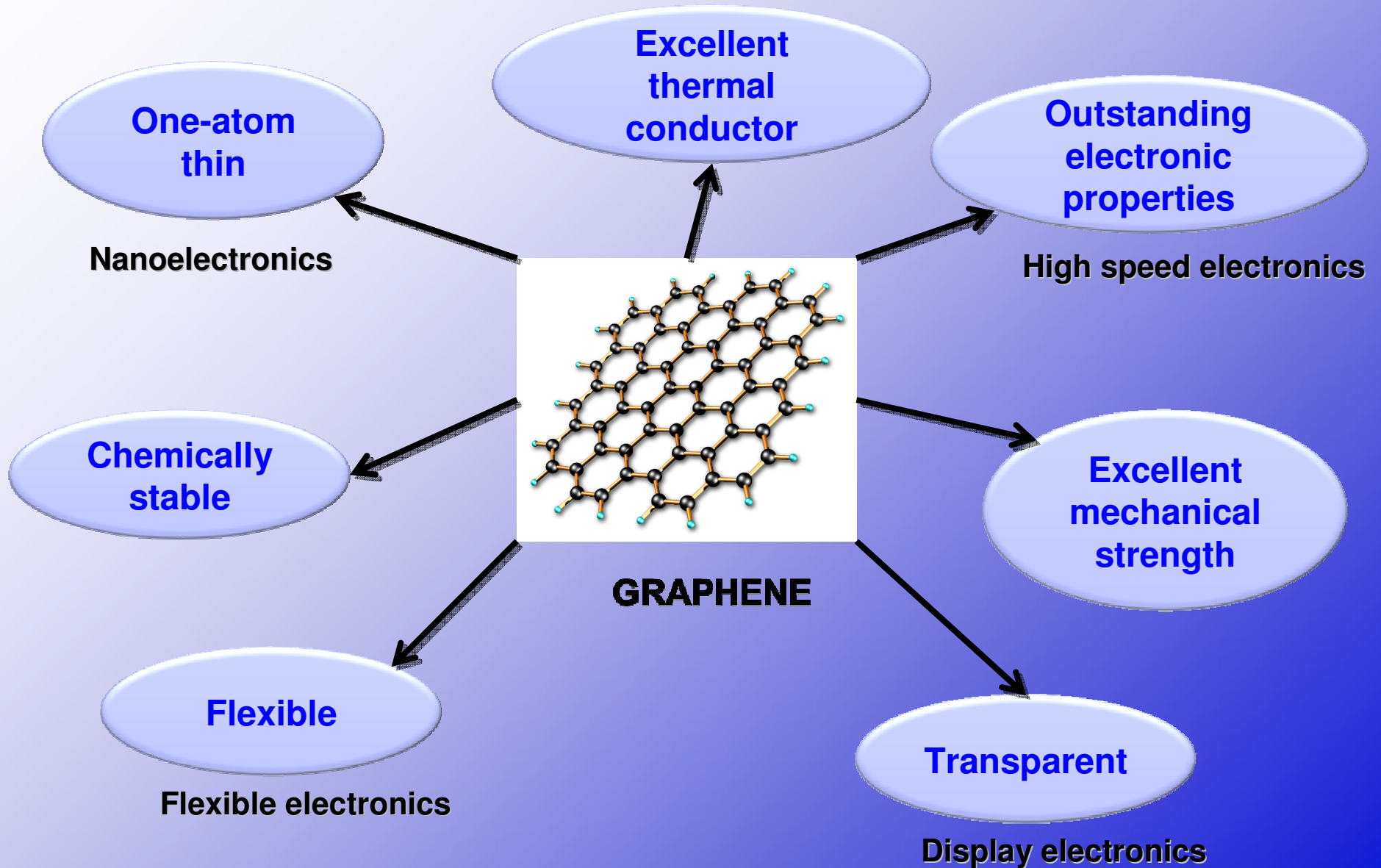


Graphene

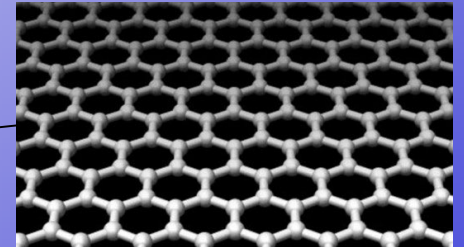
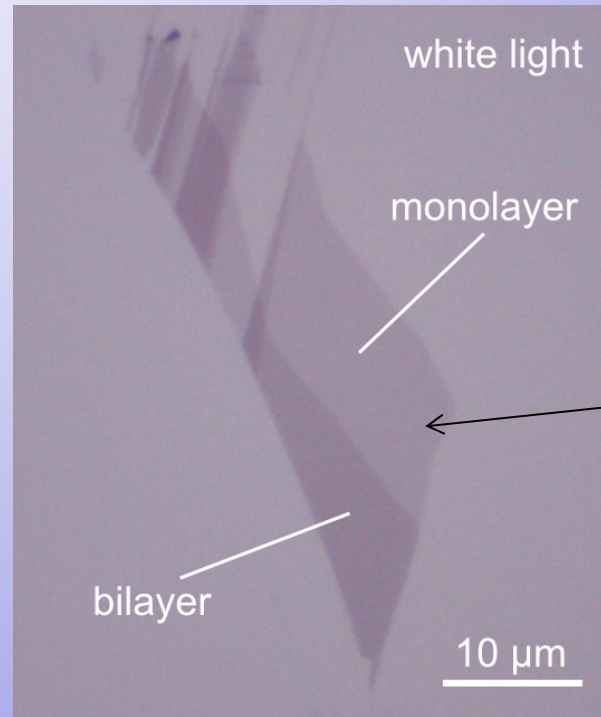
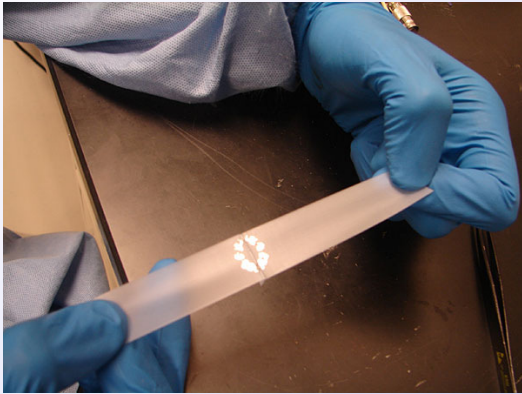
Nanotube



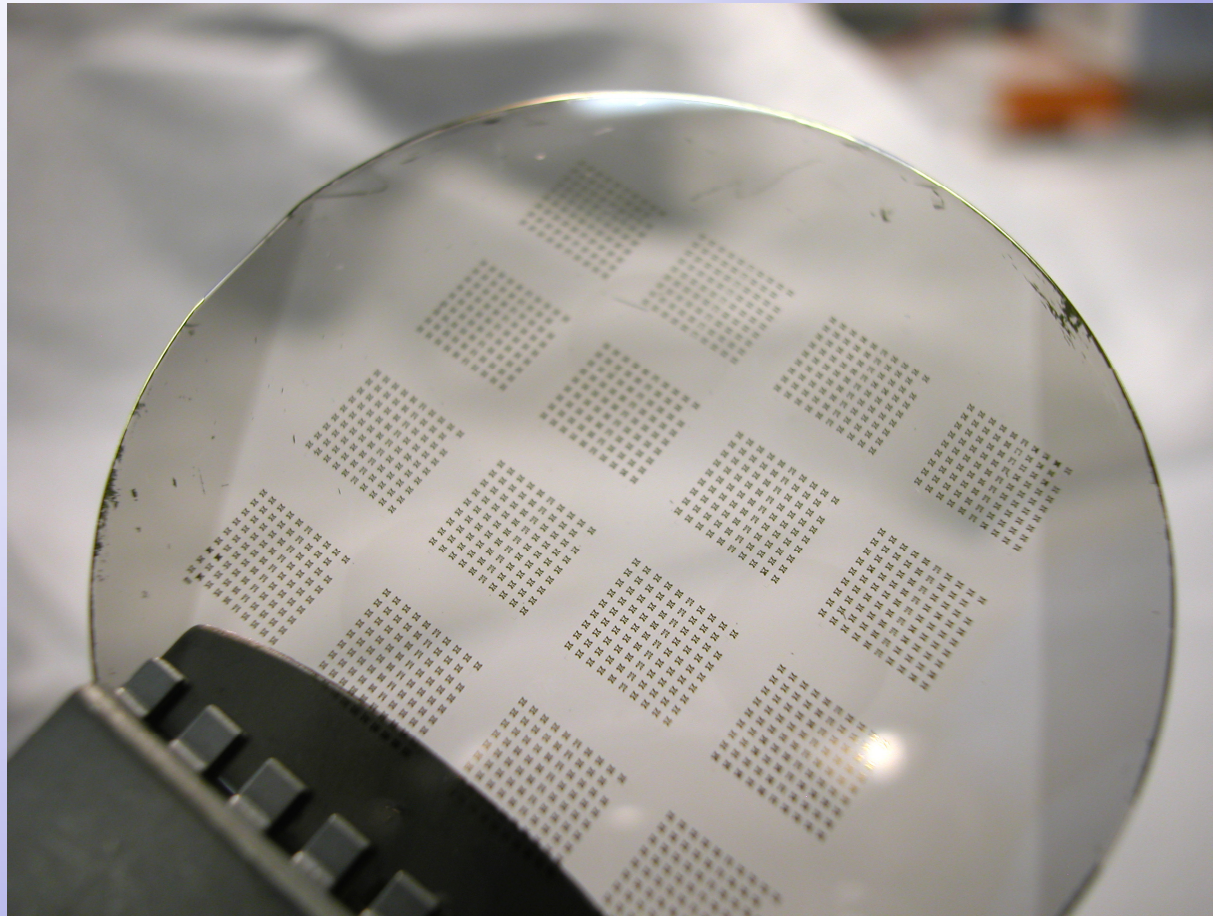
Graphene Properties and Potential



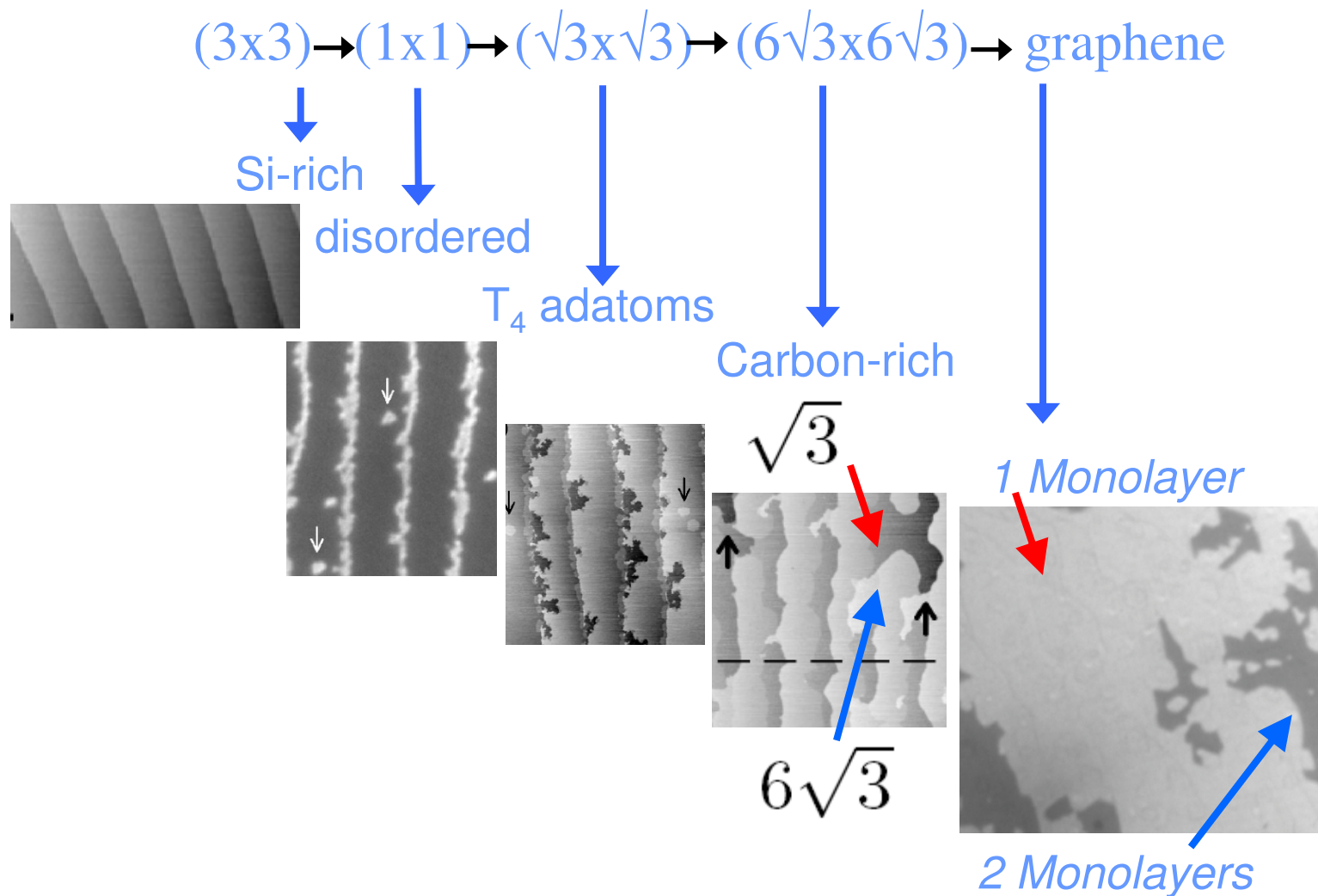
Peeling Graphene Layer from Graphite



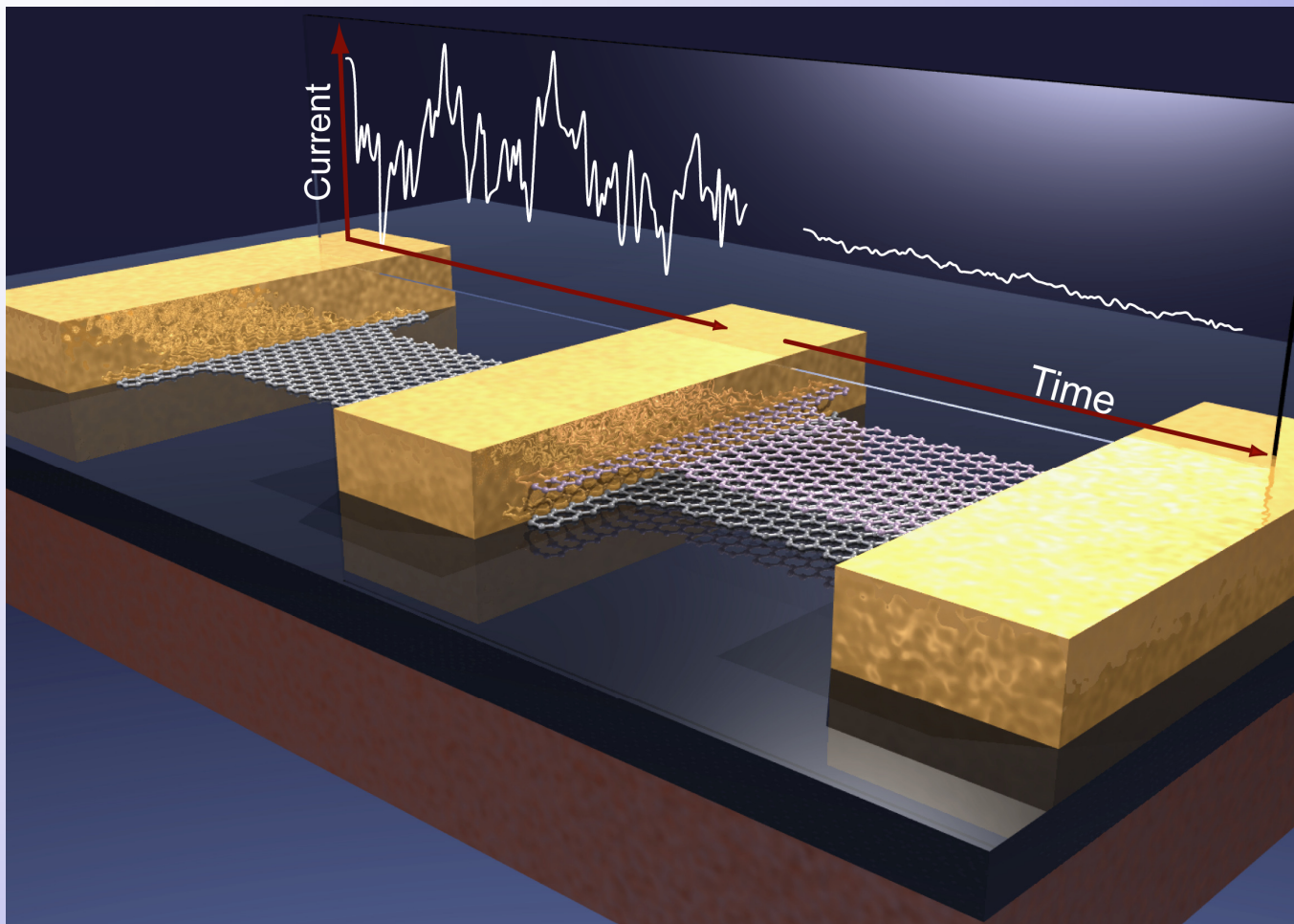
Epitaxial Graphene on a SiC Wafer



In-Situ Monitor Graphene Formation

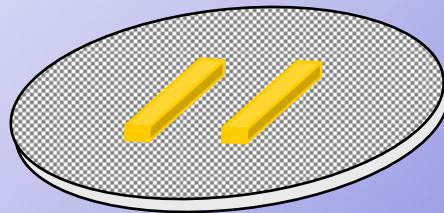
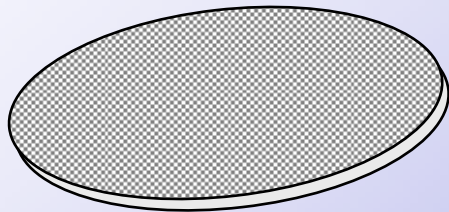


Graphene Electronics



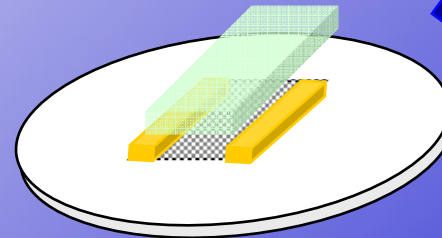
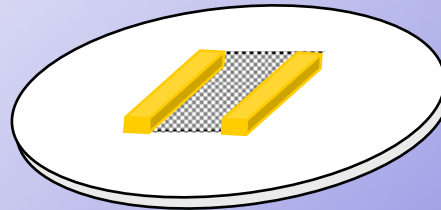
Fabrication of Graphene Transistor

Epi-Graphene wafer or
Transferred graphene



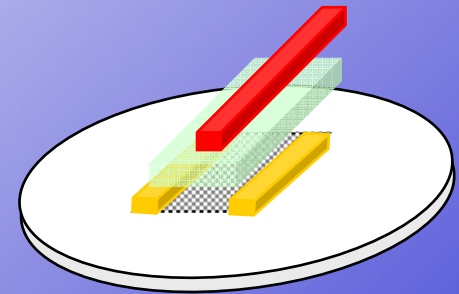
Contact electrode

Channel patterning



Gate dielectrics

Gate electrode

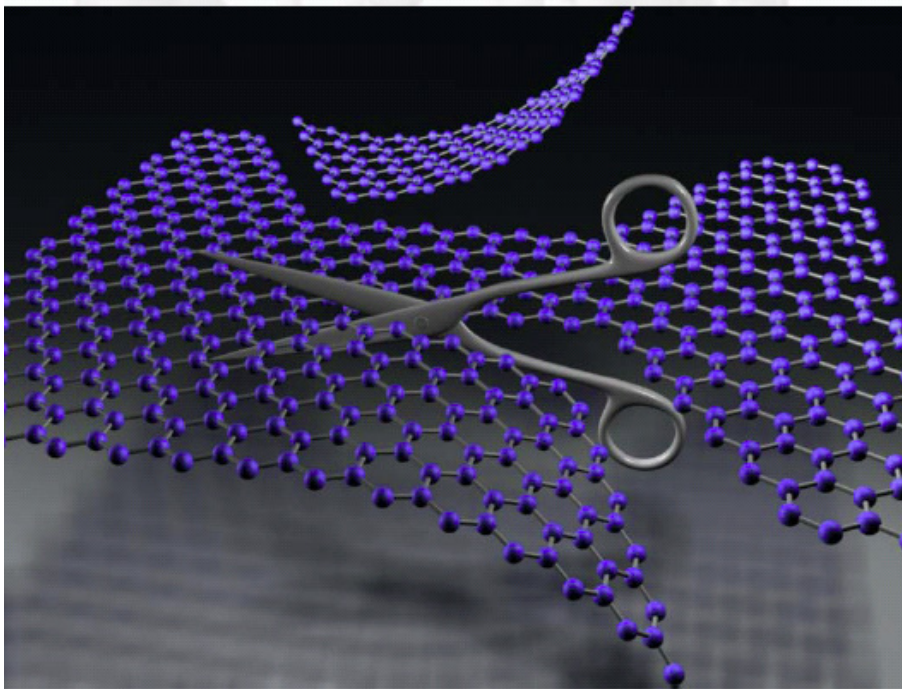


Outline

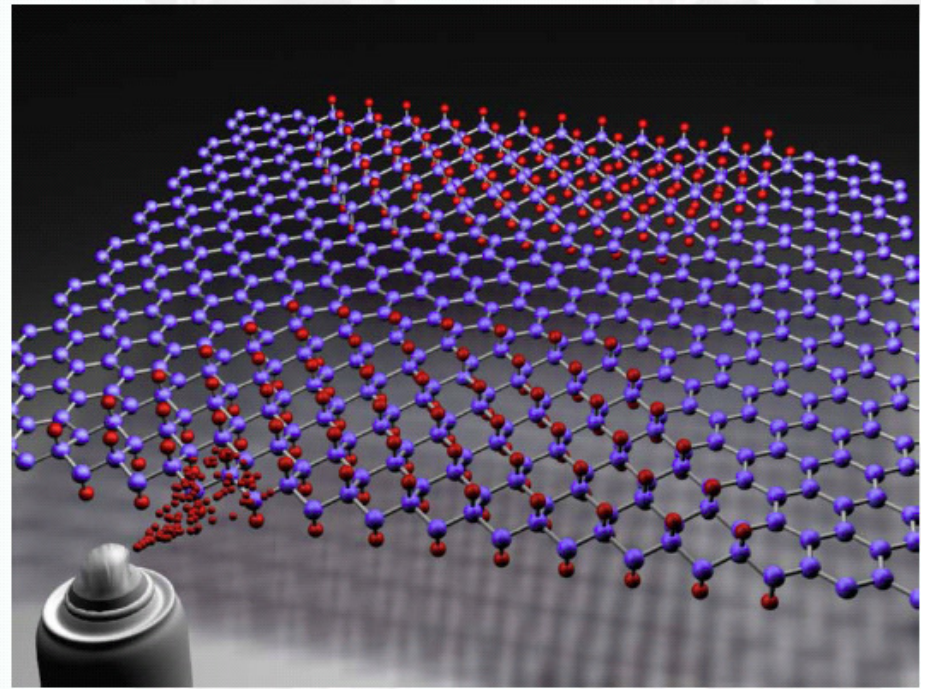
- IBM Nanoelectronics Strategy
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 - Post CMOS Carbon Electronics Opportunities
- **Applications**
- Conclusions

Atomic Layer Cutting or Painting

Nanoribbon, Quantum Dots, Quantum Point Contacts



RIE Etching



Hydrogenation

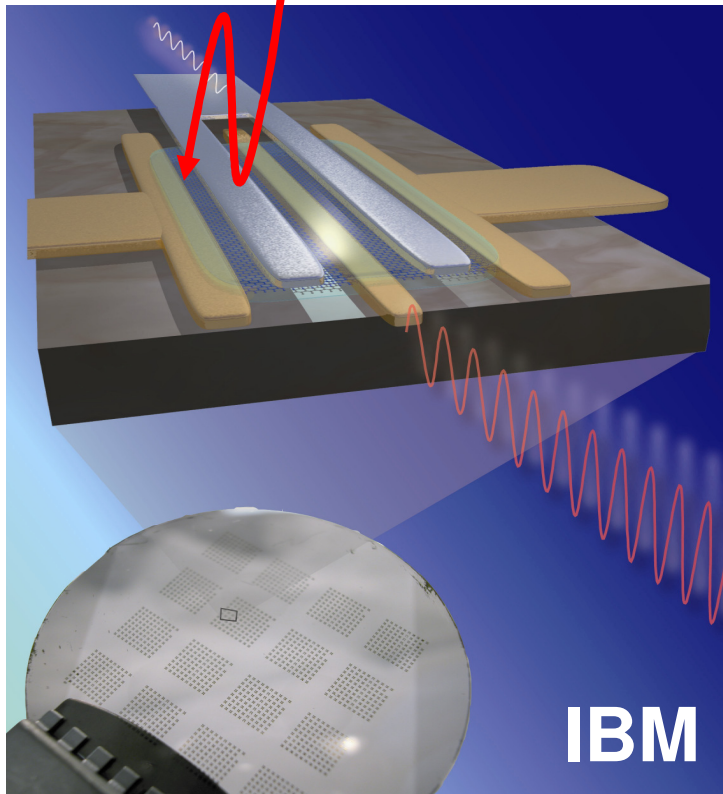
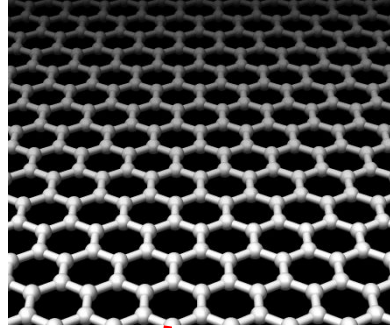
>100 GHz Graphene Devices Enable

Automobile Electronics



Adaptive cruise control radar for automobiles

Graphene

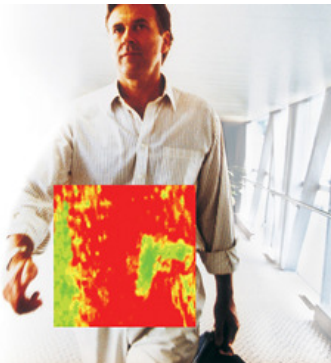


Communication



Lower power, higher resolution radar and communication systems

Security

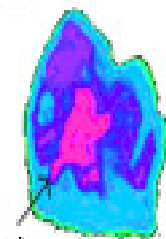


Improved weapon detection

Imaging for Health Care

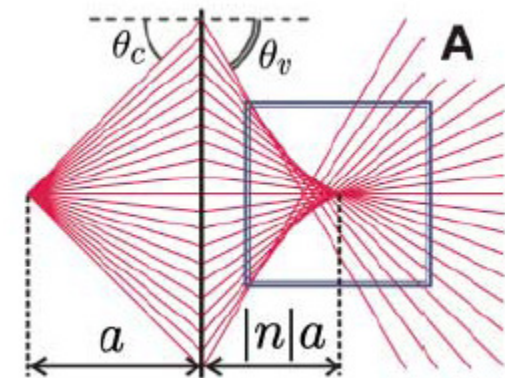
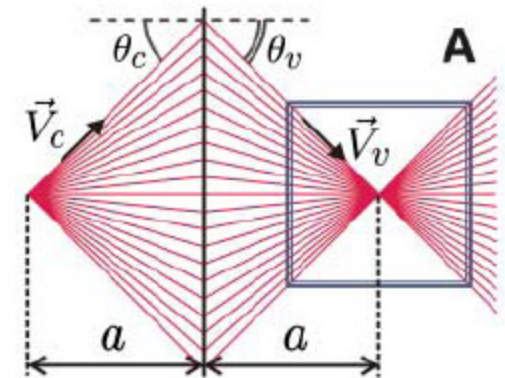
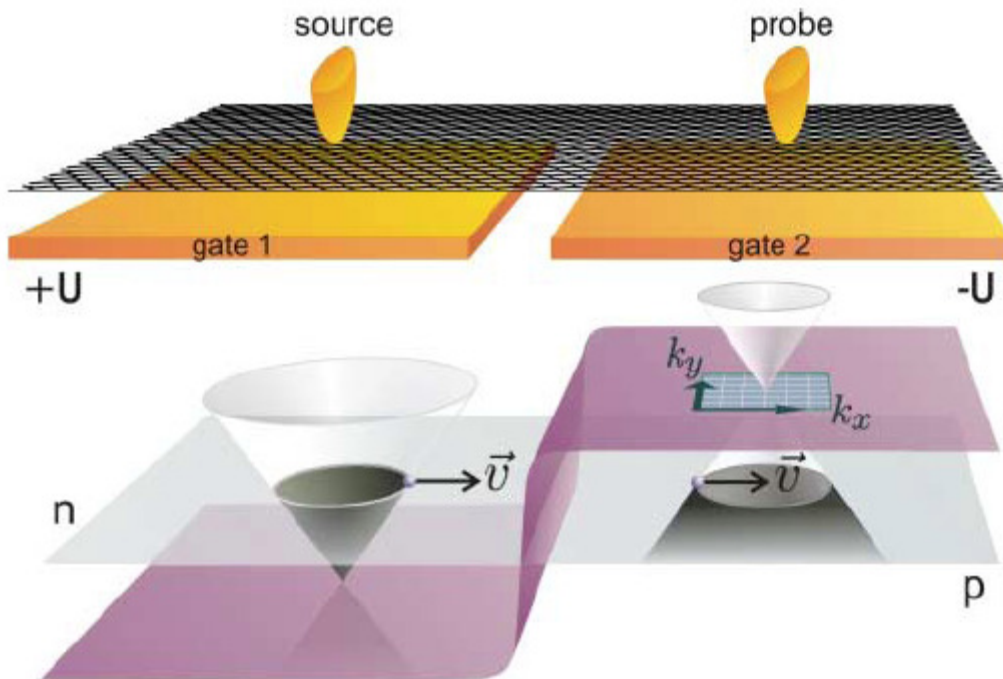
Visual Image

Terahertz Image



Cavity

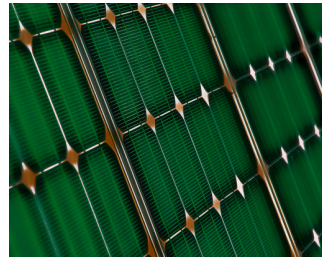
Veselago Lens Switches



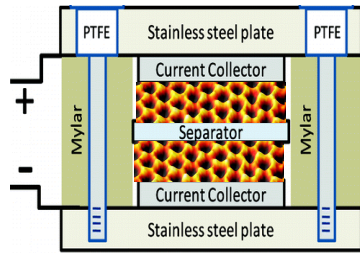
- On/Off via electron focusing
- Speed

Cheianov, Fal'ko & Altshuler,
Science (2007)

Graphene Roadmap

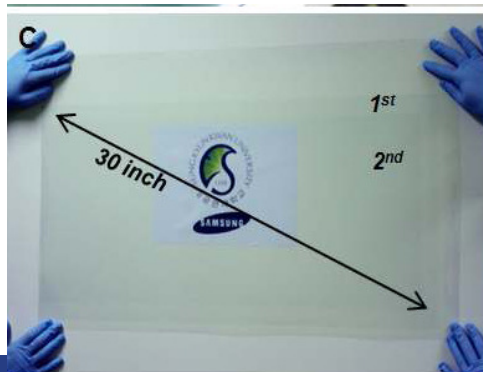


Photovoltaics



Supercapacitors

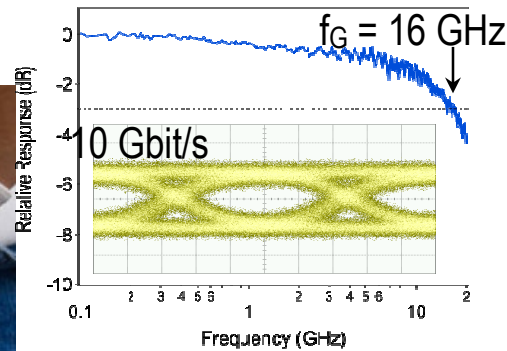
Transparent electrodes



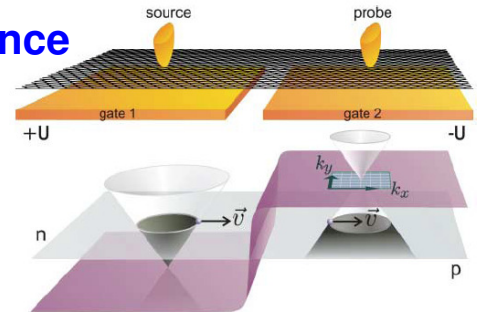
Smart Sensors



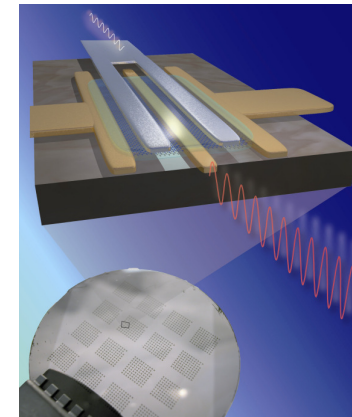
Optoelectronics Devices



High Performance Computing



Low-cost RF Circuits
Mid-performance (GHz)



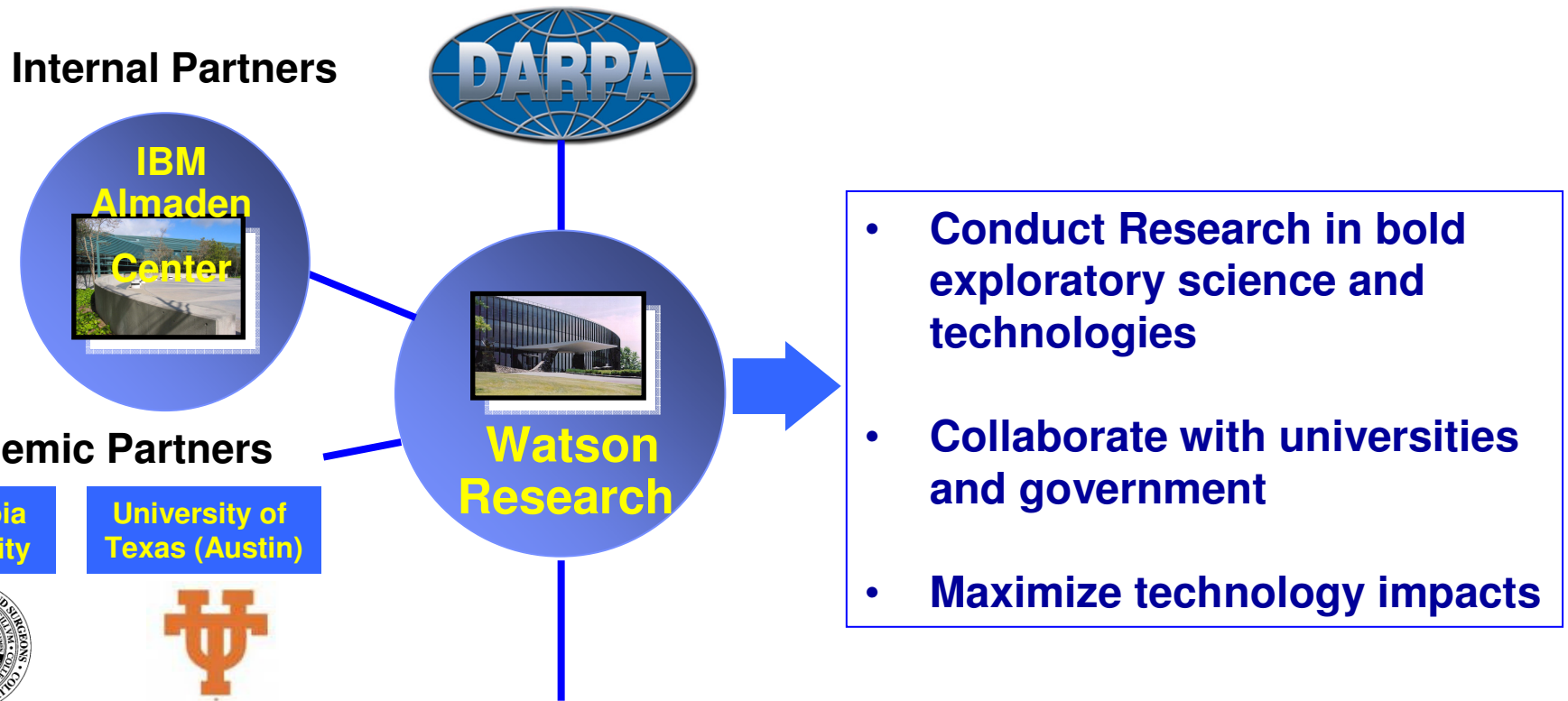
Processing Challenges

Outline

- IBM Nanoelectronics Strategy
 - Pushing Si CMOS to Limits
 - Subsystem Solutions
 - Post CMOS Carbon Electronics Opportunities
- Applications
- **Conclusions**

Graphene Research Model

Government Participation



Leverage with SRC- NRI Research Centers



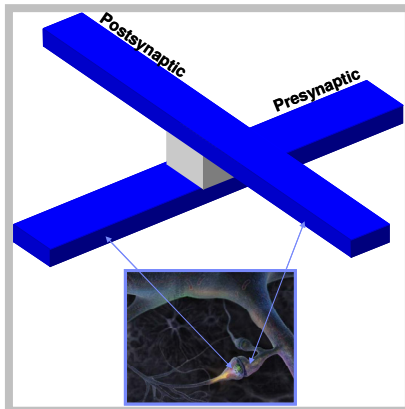
Frontiers in Energy Per Operation & Functional Diversification

Energy per Operation

Exascale Systems



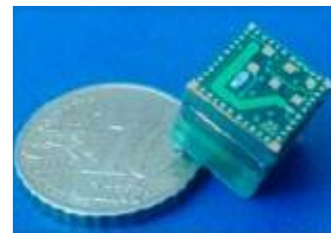
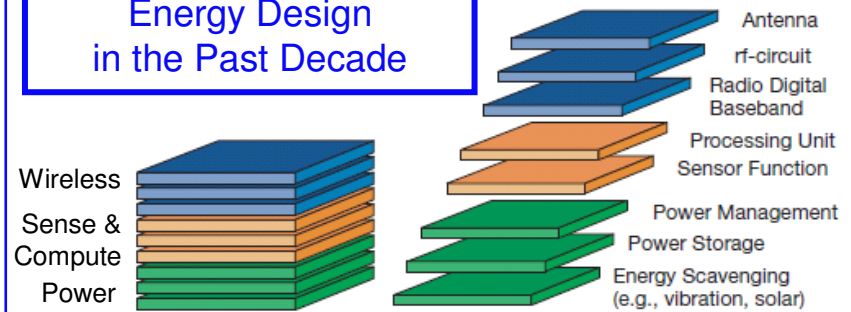
DARPA Synapse Project



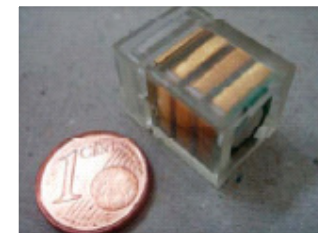
IBM's Strengths

Functional Diversification

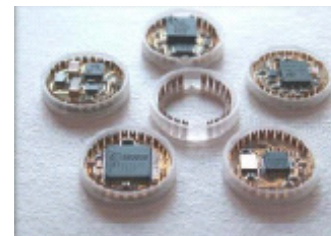
The Driver for Ultra-Low Energy Design in the Past Decade



IMEC e-Cube



UCB PicoCube



Philips Sand Module



Intel Mote

IBM New Opportunities

Frontiers of IT Nanosystem

Frontiers of IT: Vision

A new class of learning systems, architected with people as an integral and central element of the process, **to seamlessly enhance human cognition for better outcomes and a better life.**

Go beyond increased storage, better search, and more complex analytics to systems that **enable humanity to reach its greatest potential for human creativity, innovation and ingenuity.**



Learning Systems Will Impact Key Sectors of the Economy

Financial



Fraud Prevention

Retail



Revenue Maximization

Medical



Enhanced Wellness

General Business



Product Design, Launch and Time to Revenue & Profit Optimization

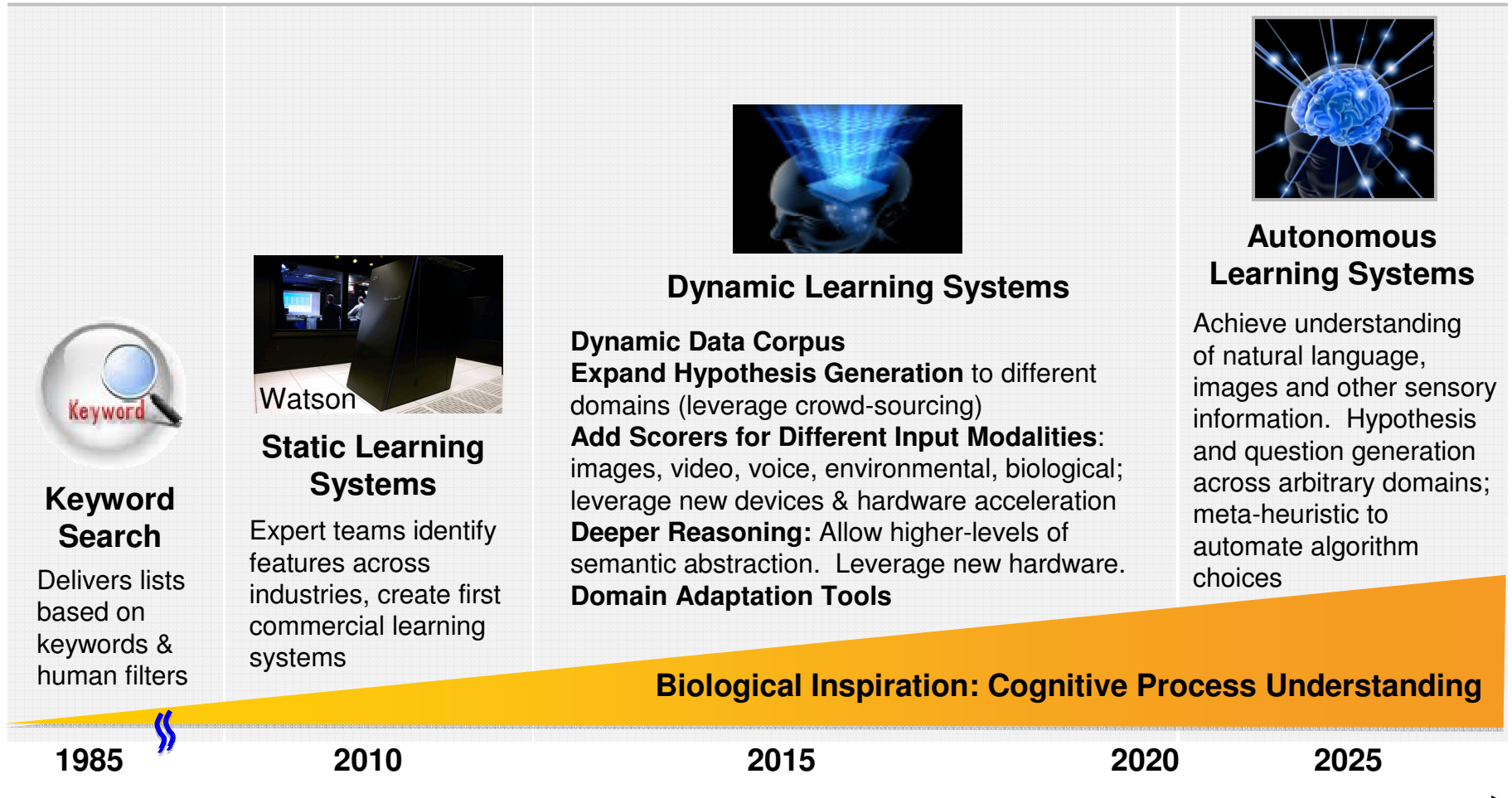
Security



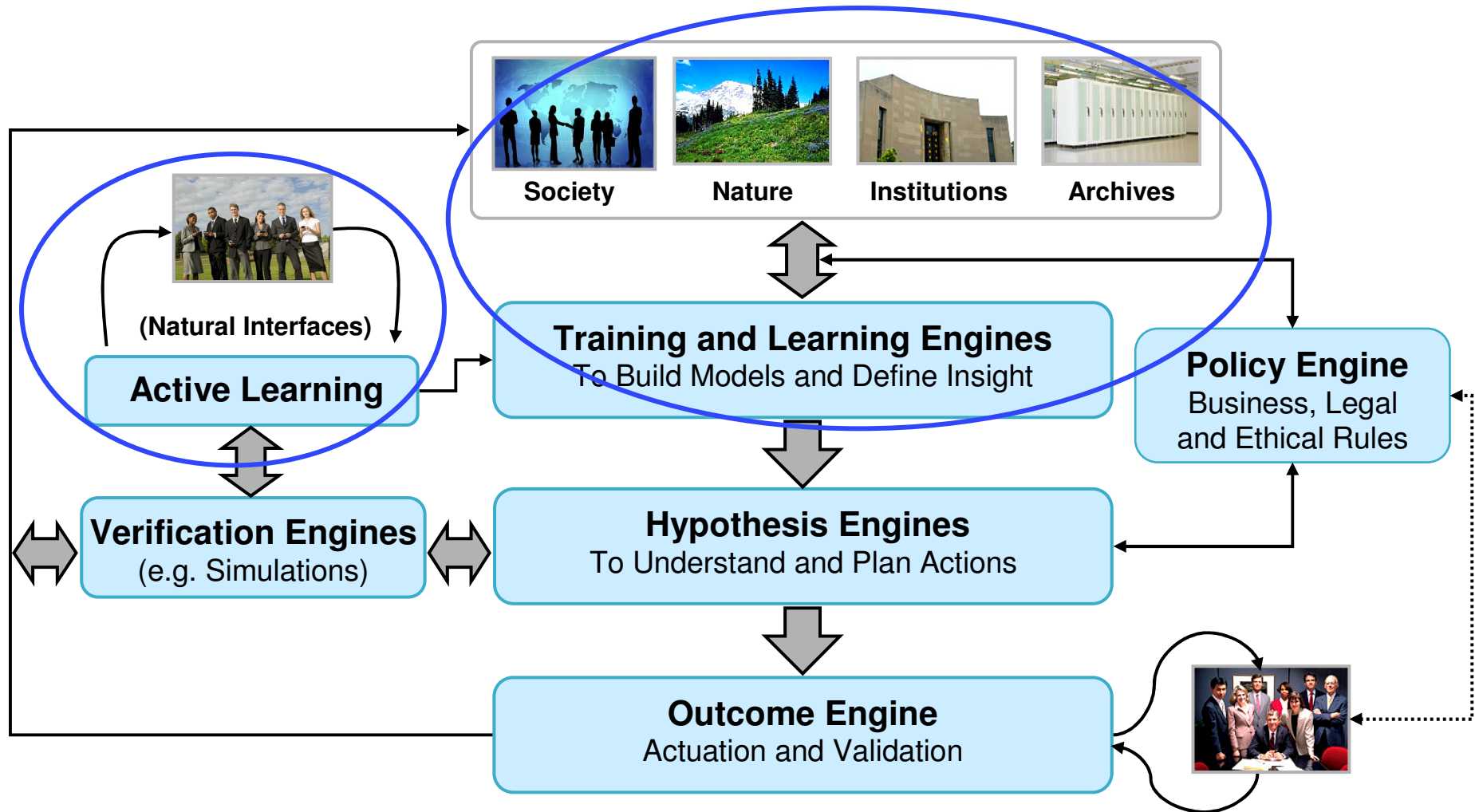
Better Security in a More Complex World

Learning Systems Roadmap to Meet the Challenge

Autonomously & accurately identify essential features across multiple domains. Learning systems must understand context to disambiguate.



Future Systems – The Learning Paradigm



Future IT System in New World

Bio Inspired Nanosystem

Deep Blue in Chess Game (1997)

IBM supercomputer famously beat the grandmaster Garry Kasparov at chess game



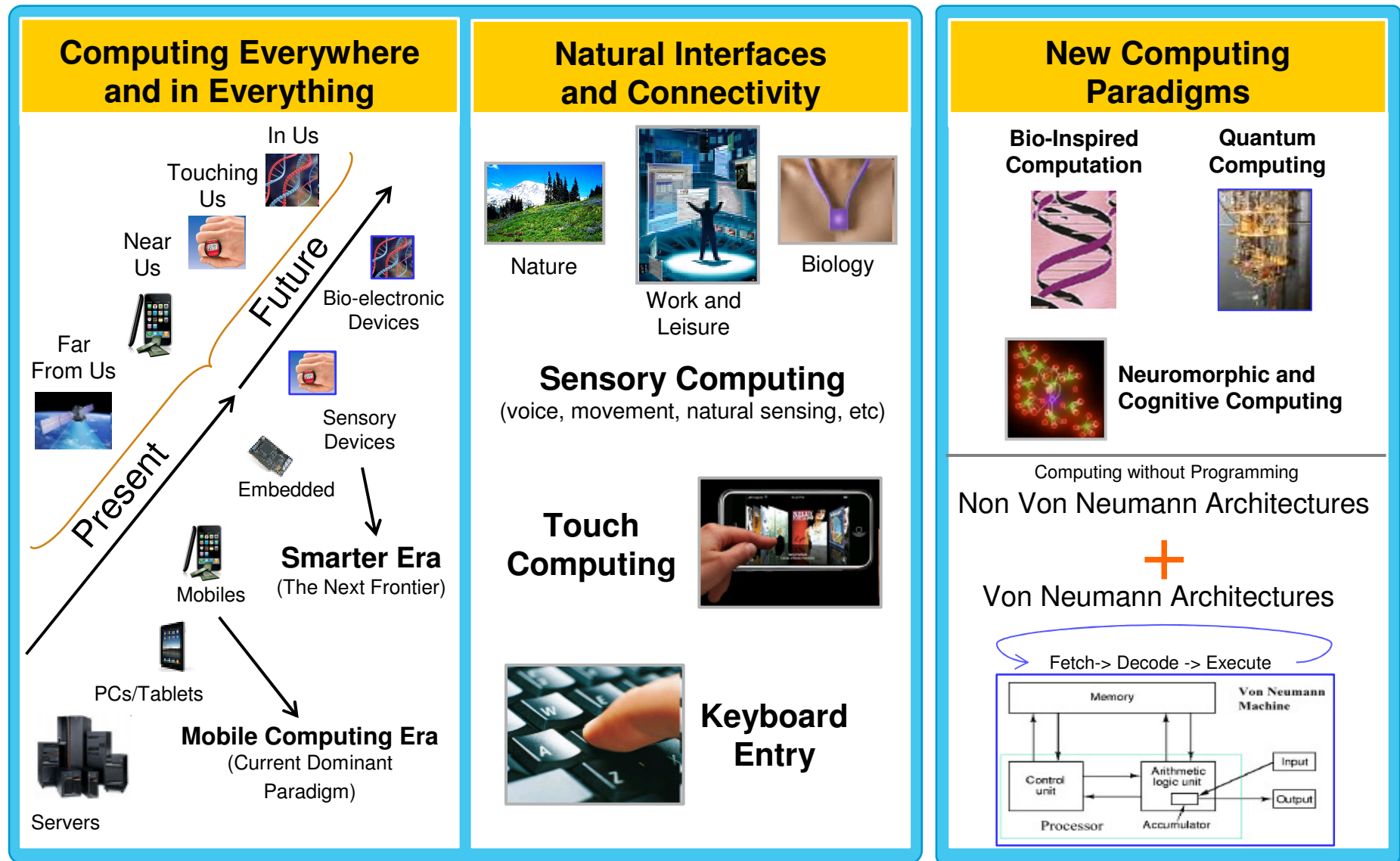
IBM Supercomputer (Watson) won Jeopardy! (2/16/2011)



Medicine, Investment (msec trading), war games, data analysis, assist judgment



Pulling it All Together: The Technology Frontiers



Inspiration from Biology

Nowhere Near Done with Technology!

Energy per Operation Frontier

The Human Brain

$P_{avg} = 20W$

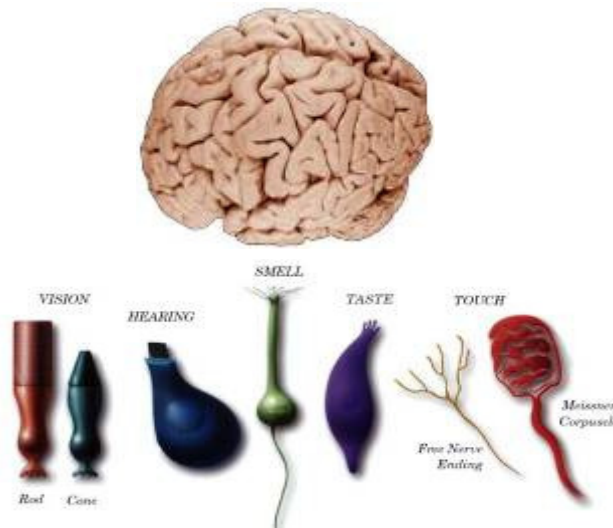
(20% of body dissipation, 2% of weight)

Power Density: $\sim 15mW/cm^3$

Avg Neuron Density: 70 million/ cm^3

10^{16} Computations/second

1-2 fJ per computation <1 aJ per operation



Thank you !

