Challenges for Design and Manufacture of Integrated Nanosystems

NSF Workshop on Design and Manufacture of Integrated Nanosystems

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Testimony Shaping NNI Reauthorization

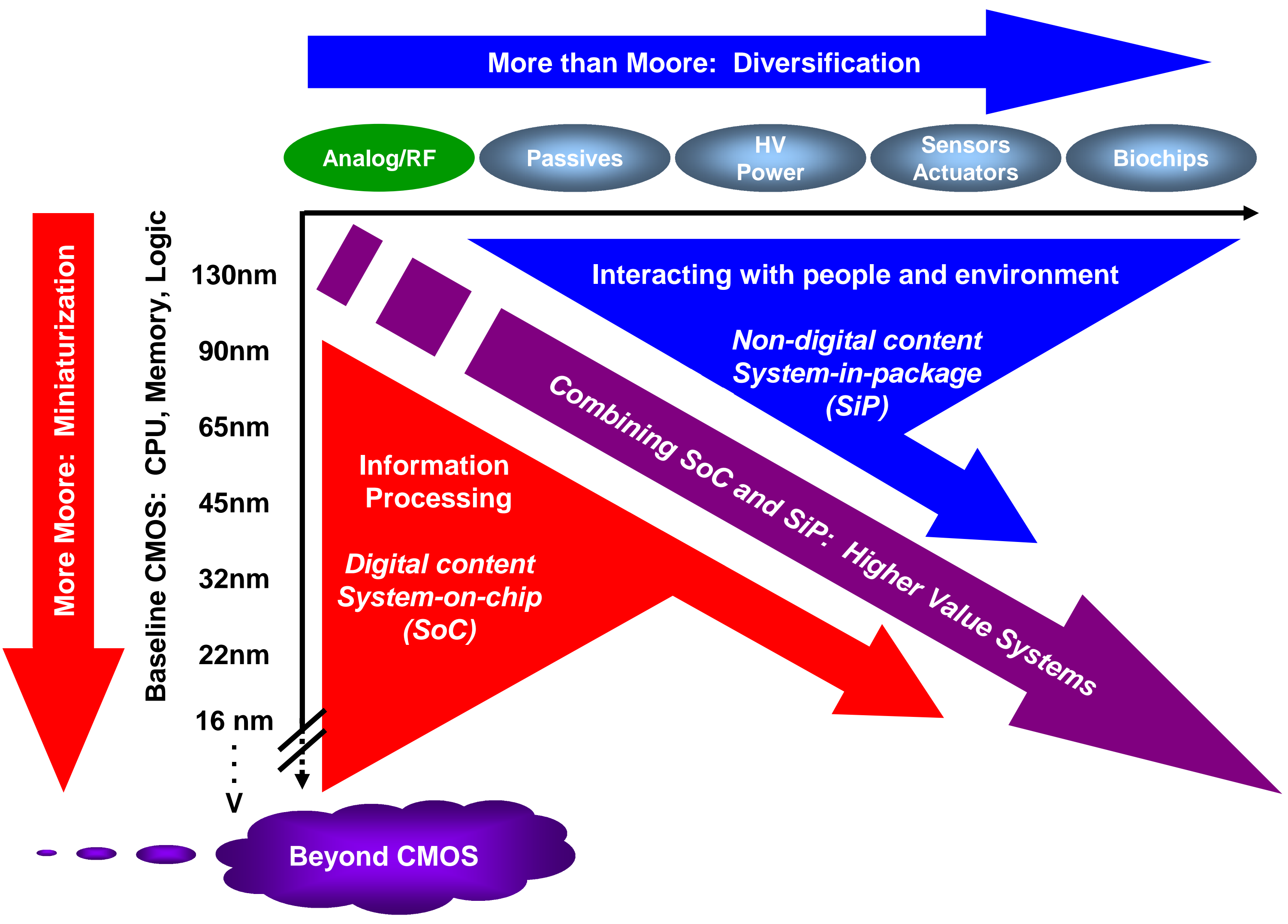
House Science and Technology Committee – April 16, 2008

Source: Texas Instruments

My Scope-Limiting Assumption for this Presentation

If the scale of integration is large, the integrated nanosystem design and manufacturing challenges are generally more diverse (i.e., worse!) cases of the challenges for VLSI integrated circuits.

Semiconductor Industry Nomenclature: Integrated Nanosystems are "More than Moore"



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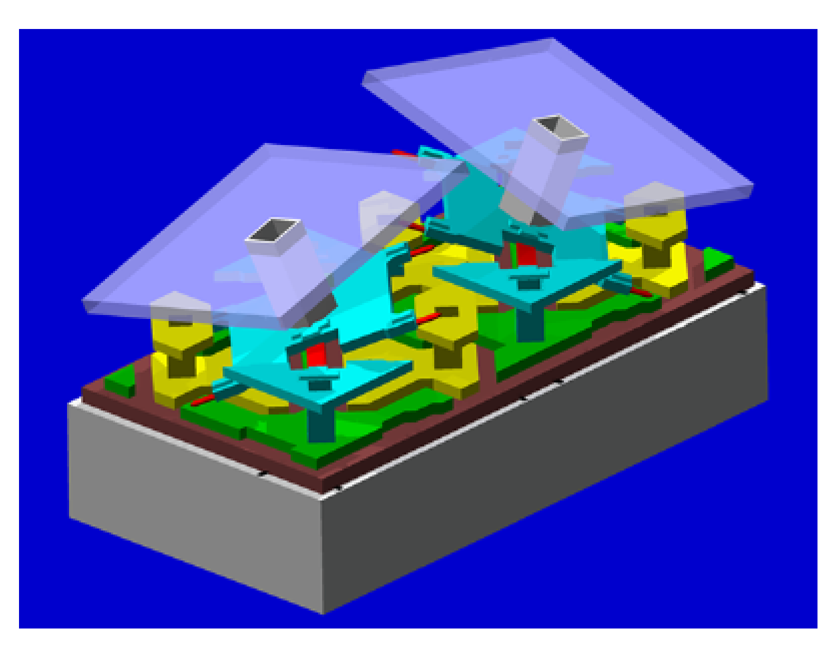
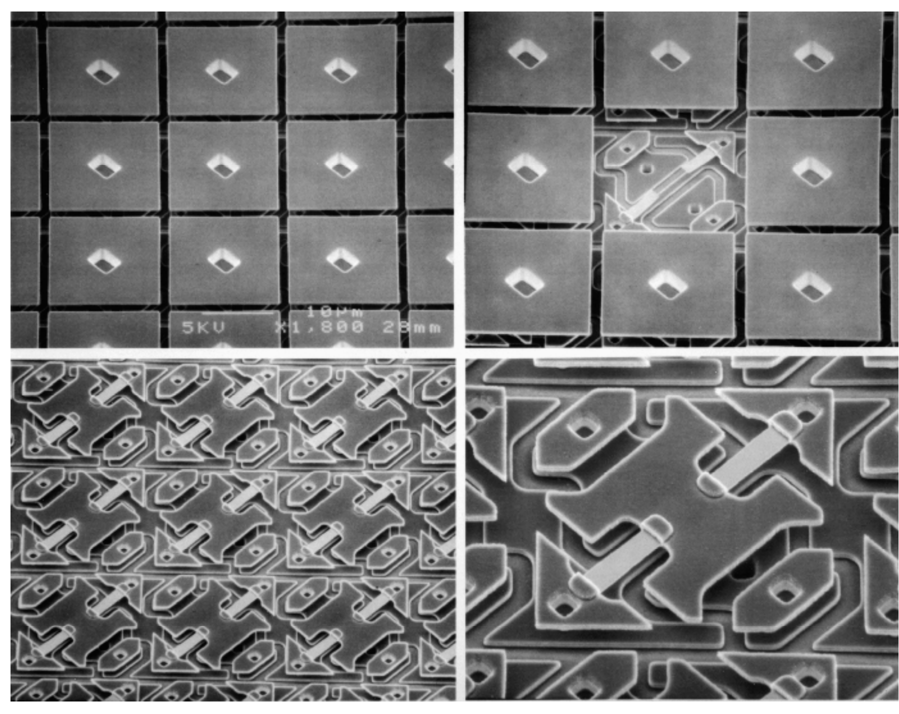
Source: 2004 ITRS Summer Conference

Early Integrated-Nanosystem Example: "Digital Micromirror Devices"

-- Extending ICs to MEMS





Source: Texas Instruments

High-Level Metrics that Could Drive Research on Nanosystem Design and Manufacturing

- **Integration Diversity** (types of elec., mech., opto, etc. functions)
- **Integration Density** (e.g., integrated functions/cm^2 or /cm^3)
- **Cost/Function** ($/gate, $/pixel, etc. in the system)
- **Functional Speed** (operations/second or throughput)
- **Power Dissipation** (both operating and standby power)
- **Capital Cost/Capacity** (capital investment $/systems/month)
- **Mfg. Cycle Time** (→ time-to-market of new or custom systems)
- **R&D Cost** (cost per new product and new technology)

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What is required for practical design and manufacture of an integrated nanosystem ?

- **BASIC DESIGN REQUIREMENTS**
  - Process Development Kit (PDK) = design rules + device models
  - Hierarchical design methodology supported by fast and accurate Design-Automation (EDA) tools
- **BASIC MANUFACTURING REQUIREMENTS**
  - Affordable and low-defect process flow, tools, and materials
  - Robust process recipes and control specifications
  - Product-optimized assembly, packaging, and test specifications

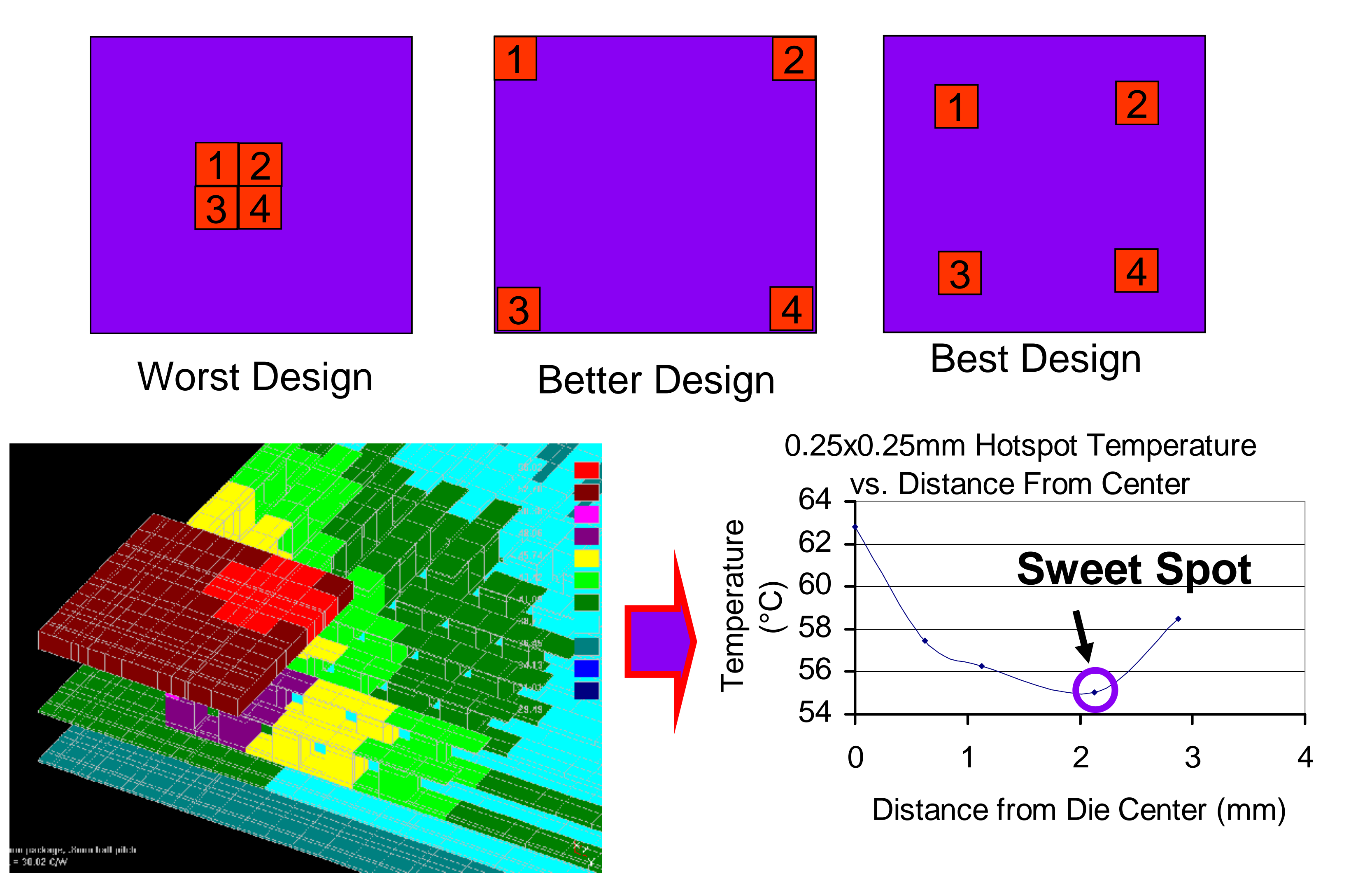
Integrated Nanosystem Design Hierarchy

Hierarchy Level	Equivalent IC EDA "Tools"
System/Architecture	C, Matlab
	We need "generalizations" of:
Library Block	VHDL, Verilog
Elementary Function	SPICE
Device/Component	OMEN, PADRE
Process/Material	TCAD (e.g., SUPREM, FLOOPS)

- *Simulation tools are required at each level*
- Expect 75% of design effort to be "verification"

For Example: Extended Thermal Simulation

Joule heating for IC → friction, … heating



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Source: Texas Instruments

Integrated-Nanosystem Cost Model

(plus 130-nm input parameters from 2002)

$$C_{unit} = \frac{Masks*C_{process/level} + C_{substrate}}{(Units/Wafer)*Yield} + \frac{Masks*C_{mask} + C_{design}}{Total\ Units} + C_{assembly\ \&\ test}$$

Yield = random defect limited = $[1 + Area*F/\alpha]^{-\alpha*Masks}$ {negative-binomial model}

F = defect density per level = 0.01 cm^{-2}

α = defect cluster factor = 5

Masks (surrogate for function/component diversity) = 25

$C_{process/level}$ = $140

$C_{substrate}$ = $500

C_{mask} = $30K

C_{design} and $C_{assembly\ \&\ test}$: treat as separate adders, case-by-case

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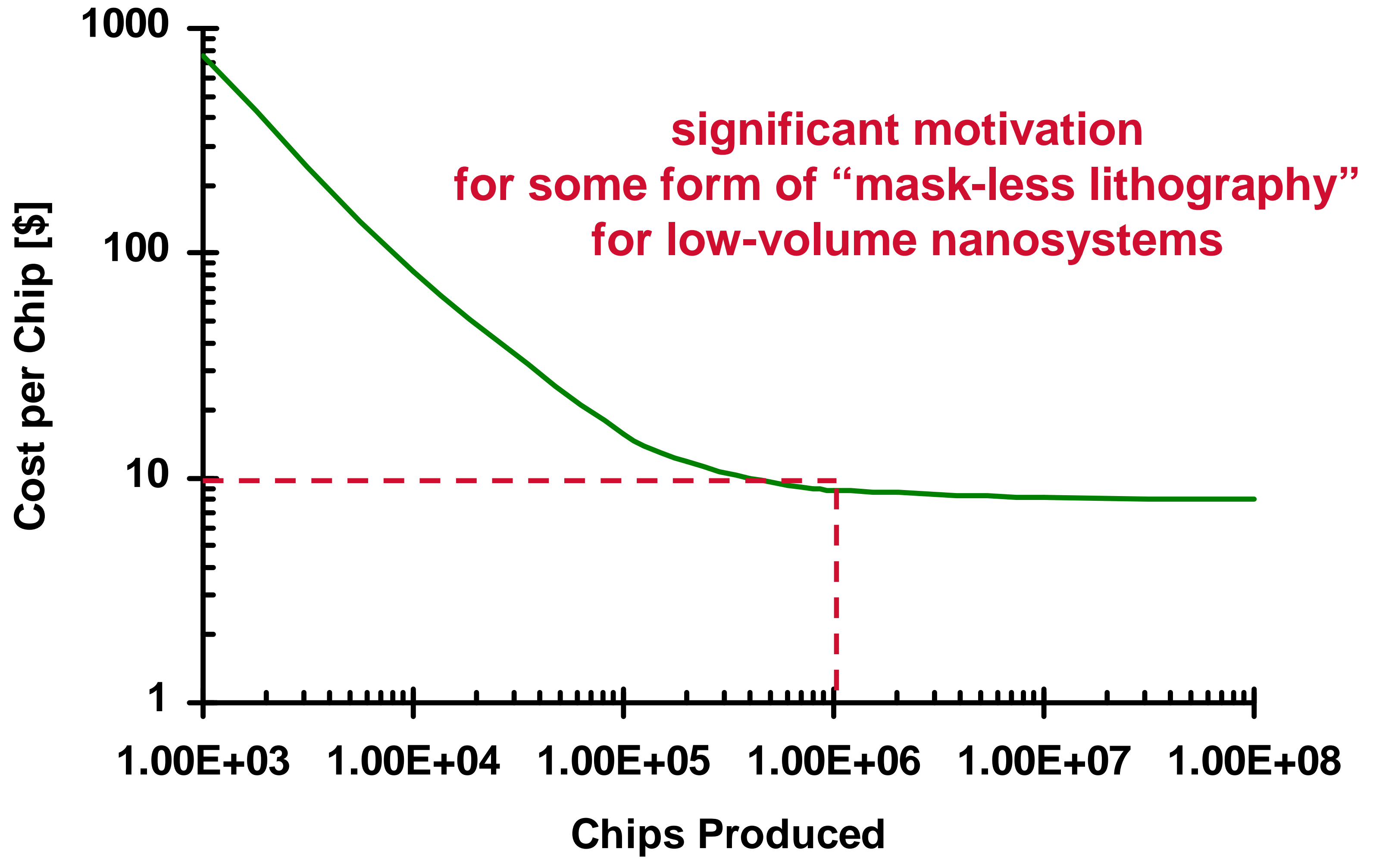
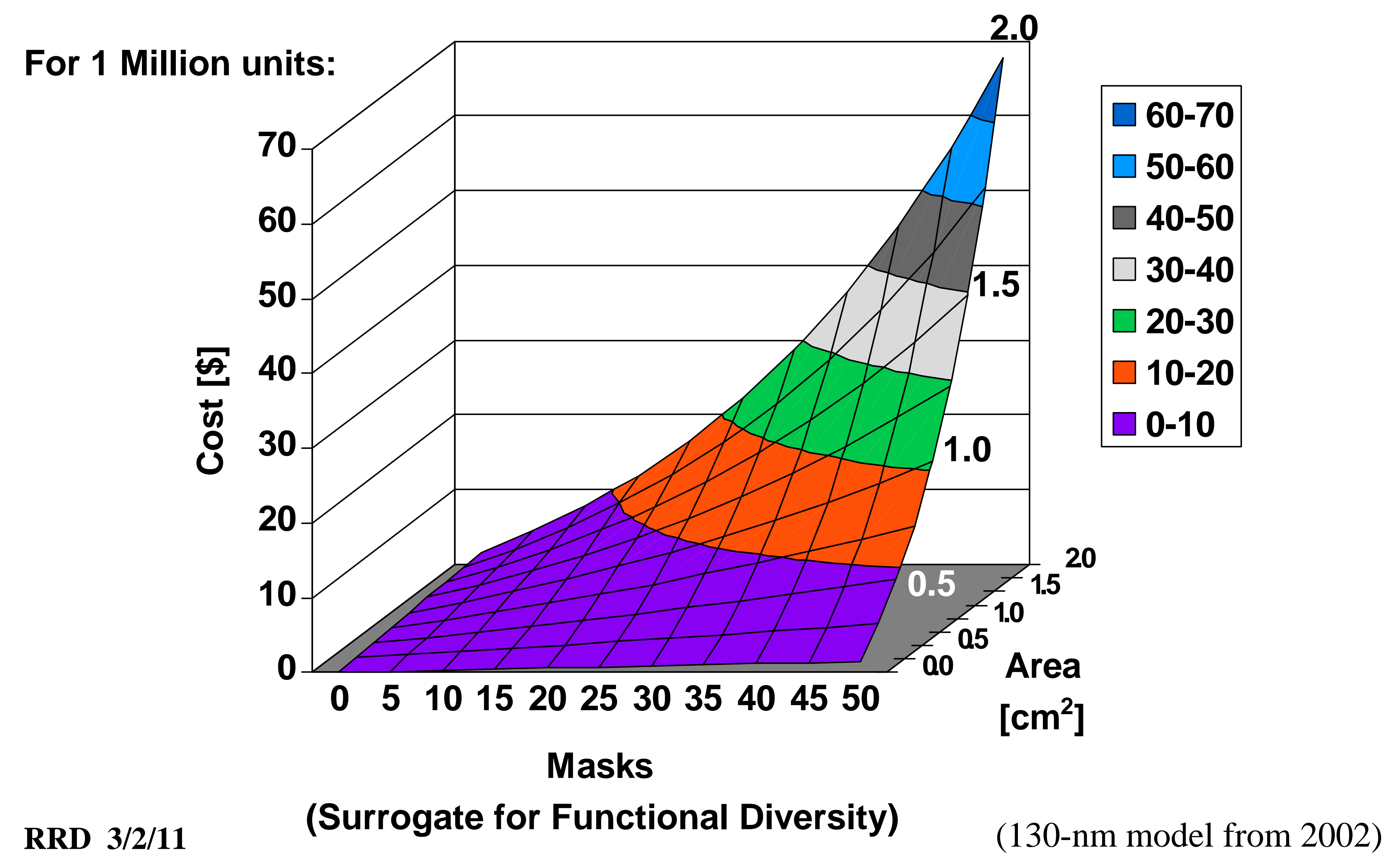
Amortization of One Fixed Cost: Masks



~ 1 million units required to get within 10% of asymptotic cost !
(and getting worse with continued scaling)

(130-nm model from 2002)

For the “Planar Mfg. Paradigm,” cost increases rapidly for large, diverse systems!



Embedded-Memory Illustration of the Integration-Diversity Cost Issue

(again: a 130-nm example from 2002)

- Suppose we wanted to create a "component-level-integrated" system with 5 million gates of logic and 128 Mbits of memory.
- The logic as a separate chip (0.4 cm^2) would cost $3.45.
- Adding the memory as SRAM would bring the chip to $49.49 (3.24 cm^2) !
- 1-T eDRAM would require much less area (0.3 μm^2 cell at 55% array efficiency ⇨ 0.7 cm^2), but at least 5 additional mask levels.
- The resulting 1.1-cm^2, 30-mask SOC would cost $12.25.
- However, note that stand-alone 128-Mbit DRAMs cost only ~ $2.40.
- Thus, it makes sense to consider alternative forms of integration, such as System-in-Package (SIP).

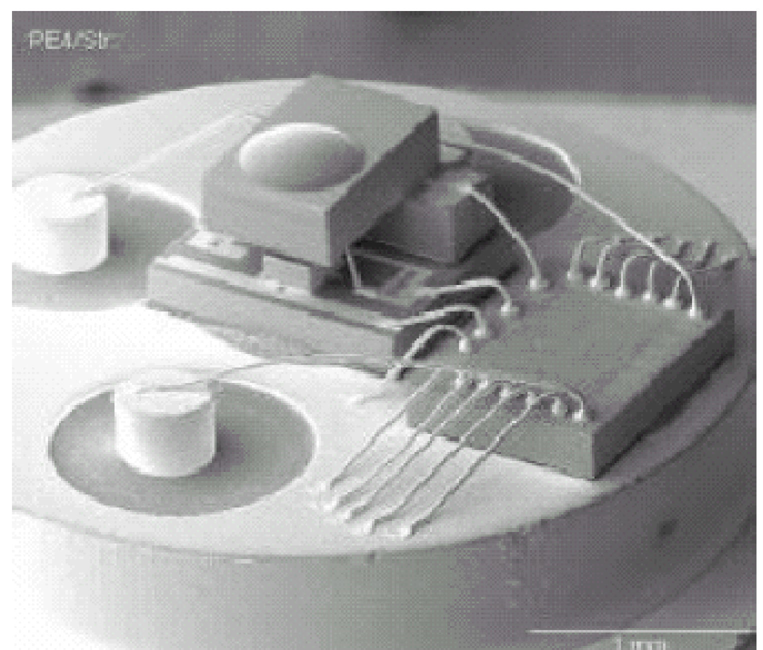
System-In-Package Research Needs

were initially addressed in the 2005 ITRS

"New system fabric types are emerging that must be incorporated into IC packaging. Requirements for these structures are being addressed in the 2005 Roadmap."

Among these new structures are:

- **MEMS**
- **Optoelectronics**
- **Bio Chips**



Source: 2005 ITRS Summer Conference

12/03 SIA Recommendations to PCAST

- **In the long term, the SIA feels that we face two grand challenges worthy of >$200M/year in new federal funding:**

(1) Scaling limits of "evolutionary lithography/thin-film manufacturing" → ***Remains "under-addressed"***

(2) Scaling limits of "charge-transport devices/interconnect"

- **We suggest that these might be overcome through new and synergistic research in the under-funded *broad areas* of:**

(1) "Directed self-assembly" of complex structures with "nanoelectronics-functionality" (computation, comm., etc.)

(2) "Beyond (classical) charge transport" signal-processing/ computational technology (e.g., based on quantum-states)

→ **"Nanoelectronics Research Initiative"**

Source: Texas Instruments